Remarks

Responses

This document is also a response to the Office Action of Restriction Requirement issued on 2006-11-20 and mailed on 2006-12-04 for US patent application 10/709920 which is invented by Chengpu Wang and which claims the benefit of the provisional patent application 60/320250.

To satisfy the Restriction Requirement:

1) Make Claims 1 to 7 depend on Claim 8.
2) Cancel Claim 138 to 169 from this application. The inventor may later present them in related patent application(s) claiming the same benefit of the original patent application.

In addition, to clarify the remaining claims:

1) Change globally the name "neighboring register" to "shared register" in order to avoid confusion with "neighboring memory element".
2) Incorporate the original Claim 8 into dependent claims to become four other independent claims.
3) Cancel some of the original claims and add some new claims.
4) Modify some of the original claims and mark them accordingly.

To help the examination process:

1) A Claim Structure section is presented on pages 52-56 of this document. The Claim Structure section shows dependence among claims, as well as a short title to summary each claim. Since this Claim Structure uses jargons to over-simplify the presented claims, it should not be treated as an official part of the application.
2) A Similar Claims section is presented on page 56. It groups similar claims together. For example, it shows that the five independent claims are similar, while becoming progressively narrower. For another example, it shows that all claims titled "Matching by priority encoder" are identical except their cited claims.
3) A paper draft is attached with this letter, to help understanding the Specification of this patent application by presenting a simplified version of the Specification.

Applicant respectfully submits that no new matter has been added by these amendments.

Claim Structure

8: broadest independent claim.
It also incorporates old Claim 2, old Claim 15 and old Claim 21.

8→2: use of the apparatus.

8→1: command bit.

8→1→7: use of command bit.

8→1→4: compliance means.

8→1→4→5: preferred compliance means.

8→3: termination means for the result means.

8→9: alternative termination means for the result means.

8→11: with instruction micro-kernel.

8→11→170: with programmable instruction micro-kernel.

8→12: use bit storage to enable memory elements.

8→14: enabled by range decoder.

8→171: carry number to be constant 1;

8→15: enabled by general decoder.

8→16: preferred maximal carry number.

8→91: parallel processing of concurrent means and exclusive means.

8→91→90: task switching.

27: 8 plus matching.
It is a combination of new Claim 8 and old Claim 27.

27→172: enabled by range decoder.

27→173: enabled by general decoder.

27→28: save match bit.

27→29: neighboring means.

27→30: matching by parallel counter.

27→30→31: use of matching by parallel counter.

27→32: matching by priority encoder.

27→32→174: matching by priority high encoder.

27→32→175: matching by priority low encoder.

27→32→33: use of matching by priority encoder.

27→32→34: matching by priority encoder and parallel counter.

27→32→34→35: use of matching by priority encoder and parallel counter.

27→32→34→36: enable by general decoder.

27→32→34→36→37: additional functionality of parallel divider.

27→32→34→36→37→38: parallel functionality of parallel divider.

27→39: status bits.

27→40: predefined matching requirement.

27→41: specified matching requirement.

27→66: simplest content comparable memory.

27→66→67: maskable content comparable memory.

27→66→73: matching by priority encoder.

27→66→73→74: use of matching by priority encoder.

27→66→73→75: matching by priority encoder and parallel counter.

27→66→73→75→76: use of matching by priority encoder and parallel counter.

80: 8 plus neighboring connections.
It is a combination of new Claim 8 and old Claim 80.

80→81: simplest content movable memory.

80→81→176: content movable memory that stores data from lowest address.

80→81→177: content movable memory that stores data from highest address.

80→81→82: preferred implementation of content movable memory.

80→81→83: moving means.

80→81→84: content moving means.

80→81→84→85: address independent means.

80→81→178: dynamic content movable memory with refresh capability.

80→81→178→179: use dynamic content movable memory with refresh capability to replace static random accessible memory.

80→81→180: content movable memory with error detection and correction capability.

92: 8 plus (a) neighboring connections and (b) matching.
It is a combination of new Claim 8, old Claim 80, old Claim 92, and old Claim 96.

92→94: predefined matching requirement.

92→95: specified matching requirement.

92→108: status bits.

92→103: enabled by general decoder.

92→103→181: matching by priority encoder and parallel counter.

92→103→181→104: additional functionality of parallel divider.

92→103→181→105: parallel functionality of parallel divider.

92→106: content comparable memory with neighboring connections.

92→106→70: use of content comparable memory with neighboring connections.

92→106→182: maskable content comparable memory with neighboring connections.

92→106→99: matching by priority encoder.

92→106→99→100: use of matching by priority encoder.

92→106→99→101: matching by priority encoder and parallel counter.

92→106→99→101→102: use of content comparable memory with neighboring connections.

92→112: simplest database memory.
It also incorporated old Claim 113.

92→112→183: database memory with bit section.

92→112→184: database memory with multiple status bits.

92→112→185: database memory with AND/OR logic bits.

92→112→115: database memory with more AND/OR logic bits.

92→112→116: matching by priority encoder.

92→112→116→186: use of matching by priority encoder.

92→112→116→187: matching by priority encoder and parallel counter.

92→112→116→187→117: use of matching by priority encoder and parallel counter.

92→112→121: database memory with incrementing capability.

92→112→121→122: use of database memory with incrementing capability.

92→112→123: math memory.

92→112→123→188: math memory with bit-section.

92→112→123→125: math memory with bitwise logic.

92→112→123→125→189: math memory with bit section.

92→112→123→125→189→190: math memory with instruction kernel.

92→112→123→191: matching by priority encoder.

92→112→123→191→192: use of matching by priority encoder.

92→112→123→191→193: matching by priority encoder and parallel counter.

92→112→123→191→193→129: use of matching by priority encoder and parallel counter.

194: 8 plus (a) 2D neighboring connections and (b) matching.

194→195: predefined 2D enabling pattern;

194→195→196: refinement of enabling pattern by matching;

194→197: enabling pattern by X and Y range decoders.

194→198: enabling pattern by X and Y general decoders.

194→199: image memory.

194→199→200: image memory with bit-section.

194→199→201: image memory with bitwise logic.

194→199→200→202: image memory with instruction kernel

194→199→203: matching by priority encoder.

194→199→203→204: matching by priority encoder and parallel counter.

194→199→203→204→131: use of image memory for 2D array.

194→199→203→204→205: use of image memory for image processing.

206: 8 plus (a) one-side neighboring connection and (b) matching.

206→207: alternative one-side neighboring connection.

206→208: enabled by range decoder

206→209: simplest content searchable memory.

206→209→210: maskable content searchable memory.

206→209→211: content searchable memory with search containing wild datum in a datum stream.

206→209→212: matching by priority encoder.

206→209→212→213: use of matching by priority encoder.

206→209→212→214: matching by priority encoder and parallel counter.

206→209→212→214→215: use of matching by priority encoder and parallel counter.

Similar Claims

The following claims are identical except their respective cited claims:

Enabled by range decoder:
14 172 208 197 (slightly different with others)

Enabled by general decoder:
15 36 103 173 198 (slightly different with others)

Matching by priority encoder:
32 73 99 116 191 203 212 174 175 (slightly different with others)

Matching by priority encoder and parallel counter:
34 75 181 187 193 204 214

Additional functionality of parallel divider
37 104

Parallel functionality of parallel divider
38 105

Status bits:
39 108 184

With bit-wise logic
125 201

The following claims are similar:

Independent claims:
8 27 80 92 194 206

Array management:
2 74 76 100 102 117 129 186 192 213 215

Mini-processor
106 112 199

With bit-section:
183 188 189 200
